ABSTRACT OF THE DISCLOSURE

An image processor has a transfer control section that transfers a sequence of image processing and data for image processing to be added or updated from a host buffer to program RAM and data RAM. The host buffer receives the sequence of image processing and data for image processing to be added or updated transferred from a process controller, and temporarily stores the sequence and the data during idle cycle time that a processor array section does not execute image processing. The transfer control section provides controls for transfer so that the sequence of image processing and data for image processing to be added or updated are split into blocks for a plurality of transfer times, and the blocks are transferred from the host buffer to the program RAM and the data RAM.